REMARKS

Claim Objections

Claim 1 recited the limitation "a second portion" and "a second partial circumferential part". The Examiner asserted that there was insufficient antecedent basis for this limitation in the claim. As claim 1 is not at issue in the present application, the Applicant assumes that the Examiner was referring to claim 29 and will respond as such. The Applicant traverses the objection and believes that the recited limitations of claim 29 have sufficient antecedent basis. However, the Applicant has amended claim 29 to more clearly define the claimed subject matter.

Rejection Under 35 U.S.C. § 103

Claim 29 was rejected under 35 U.S.C. §103(a) as being unpatentable over Dennison '666 (U.S. Patent No. 5,362,666).

Referring to claim 29, the claim as amended recites, in part, "masking a first partial circumferential portion of said insulating layer" and "etching a second partial circumferential portion of said insulating layer from a partial circumferential part of said exterior surface to expose the part of said exterior surface." Applicant respectfully submits that this process of masking and the subsequently recited etching is neither taught nor disclosed in Dennison '666, as the cited photo resist layer 44 of Dennison '666, Fig. 4, is formed within the container 41 and in contact regions 38 and 40. Applicant submits therefore that Dennison '666 does not teach or suggest masking all or a portion of the exterior surface of the container 41. (See Dennison '666, Figs. 4-5 and col. 10, ln. 39-42). Further, in Dennison '666 the cited insulating layer 32 of Fig. 4 is shown covered by storage poly/first conducting layer 42 in relation to photo resist layer 44 and thus is unetchable. (See Dennison '666, Fig. 4 and col. 10, ln. 39-66).

Additionally, Applicant respectfully submits that the process of claim 29, namely masking a first partial circumference and subsequently etching a second partial circumference is neither taught nor disclosed in Dennison '666, as Dennison '666 performs an etch to remove

the supporting insulator 32 to a uniform depth around the entire exterior circumference of the container 41. (See Dennison '666, Figs. 4-5 and col. 10, ln. 39-66).

Applicant respectfully maintains that Dennison '666 does not teach or suggest a process for making a container capacitor having a cup-shaped bottom electrode having an exterior surface with a first partial circumferential portion of the exterior surface covered by an insulating layer and a second partial circumferential portion of the exterior surface exposed, wherein the exposed second partial circumferential portion and an interior portion of the cup-shaped bottom electrode are covered by a dielectric layer on which a conductive layer is placed, forming a top electrode. The process comprising the steps of providing a cup-shaped bottom electrode, providing an insulating layer around and in contact with an exterior surface of said cup-shaped bottom electrode, masking a first partial circumferential portion of said insulating layer, etching a second partial circumferential portion of said insulating layer from a partial circumferential part of said exterior surface to expose the part of said exterior surface, depositing a dielectric layer on said part of said exterior surface, and depositing a conductive layer on said dielectric layer.

Claim 67 was rejected under 35 U.S.C. §103(a) as being unpatentable over Dennison '666 (U.S. Patent No. 5,362,666) in view of Dennison '725 (U.S. Patent No. 6,331,725).

Applicant respectfully submits that claim 67 recites, in part, "etching a second portion of the insulating layer from a first region of the exterior surface to expose the first region of the exterior surface, such that the insulating layer remains in contact with an entire vertical height of a remaining region of the exterior surface." Applicant respectfully submits that this differs from the structure of Dennison '666, which in etching exposes all or a part of a vertical depth of the bottom electrode around the entire circumference of the electrode.

Additionally, Applicant respectfully submits that Dennison '666 does not teach or disclose a masking layer over the insulating layer 32, as disclosed in Applicant's claim 67, but discloses an etch stop layer 30 that resides under the insulating layer 32 to stop the etching

process once the insulating layer 32 has been etched away. (See Dennison '666, Figs. 4-5 and col. 10, ln. 15-66). Further, Applicant submits that the etching process disclosed by Dennison '666 is a timed etch that does not rely on a mask layer or etch stop layer in its removal of the insulating layer. (See Dennison '666, Fig. 5 and col. 10, ln. 54-56).

Applicant also submits that the etch stop or hard mask layer 31 of Dennison '725, while over an insulating layer 30, is a permanent feature of a three dimensional capacitor DRAM array, separating the container capacitor layer and the wordline/bitline layer of the DRAM array, and does not function as a mask layer. (See Dennison '725, col. 1, ln. 15-36). Furthermore, it is applied in a uniform layer and must be masked and etched in its own right to provide openings through it in a complex multi-step process. (See Dennison '725, Figs. 1-5, col. 4, ln. 21-67). As such, Applicant submits that Dennison '725 does not disclose a process mask but a etch stop layer and that one skilled in the art would be motivated away from utilizing such an etch stop/hard mask layer as a process mask.

CONCLUSION

Applicant believes that all of the claims are in condition for allowance and respectfully requests a withdrawal of the rejections and allowance of the Application. If the Examiner has any questions regarding this application, please contact the undersigned attorney at direct dial (612) 312-2207.

Respectfully submitted,

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MARKED-UP VERSION OF AMENDMENTS

IN THE CLAIMS

29. (Twice Amended) A method for forming a container capacitor, comprising the steps of:

providing a cup-shaped bottom electrode;

providing an insulating layer around and in contact with an exterior surface of said cup-shaped bottom electrode;

masking a first partial circumferential portion of said insulating layer;

etching a second partial circumferential portion of said insulating layer from a[second] partial circumferential part of said exterior surface to expose the part of said exterior surface;

depositing a dielectric layer on said part of said exterior surface; and

depositing a conductive layer on said dielectric layer.